Circuits, Uniformity and non-deterministic Turing Machines

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SAS, Isaac Newton Institute, April 17, 2012

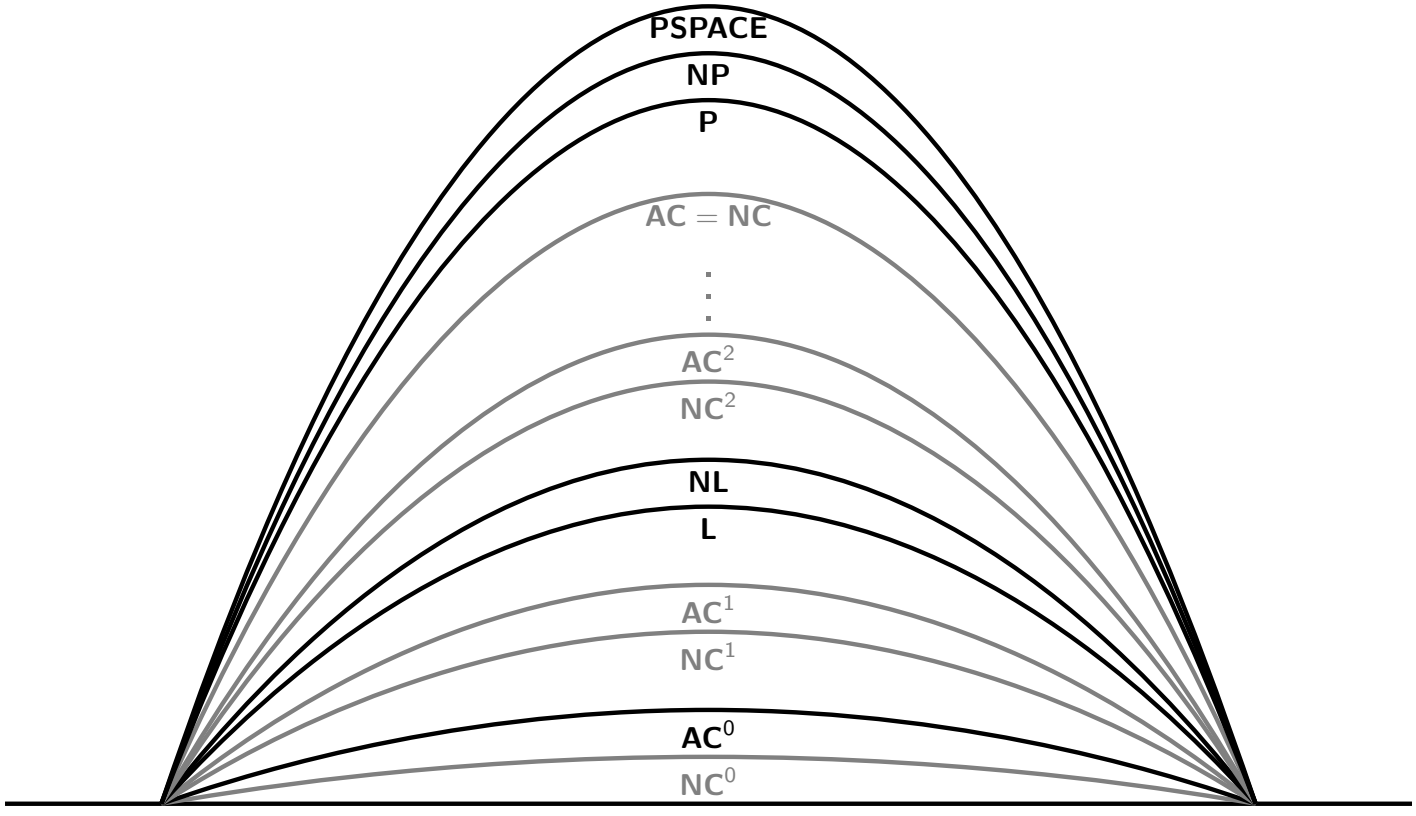
Terminology

A problem or a language $L \subseteq \{0,1\}^*$. $f(w) = 1$ if $w \in L$.

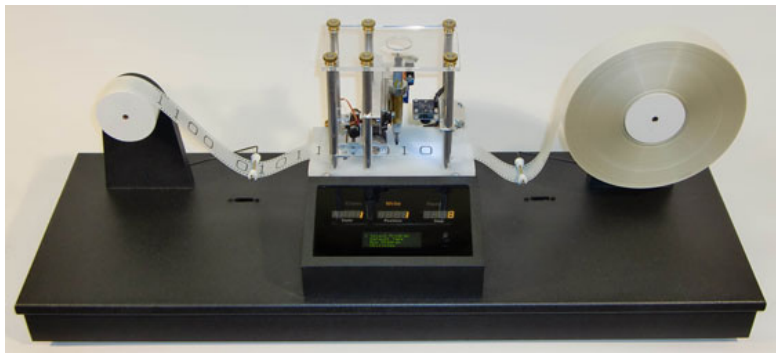
- PATH: in a dag, is there a path from node s to node t.
- PARITY: are there an odd number of 1s in a string.

Some complexity classes

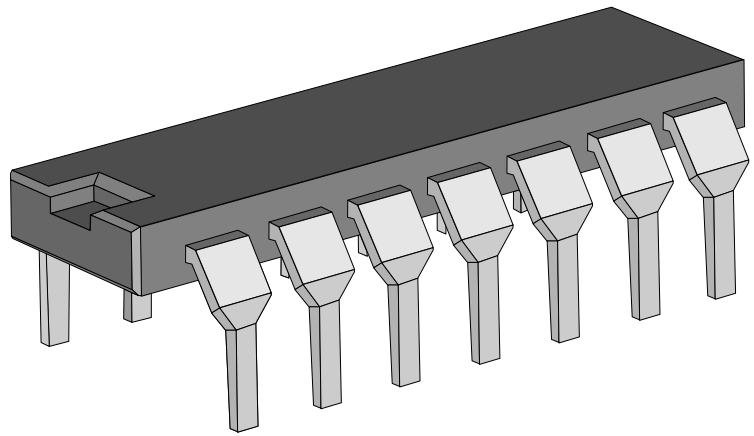
- $\mathbf{L} \subsetneq \mathbf{PSPACE}$
- $\mathbf{AC}^0 \subsetneq \mathbf{NC}^1$



Fixed size devices

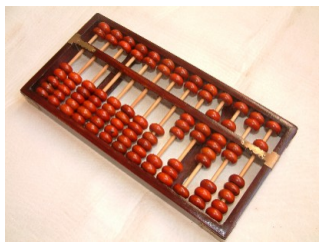


[1]



[1] http://aturingmachine.com/

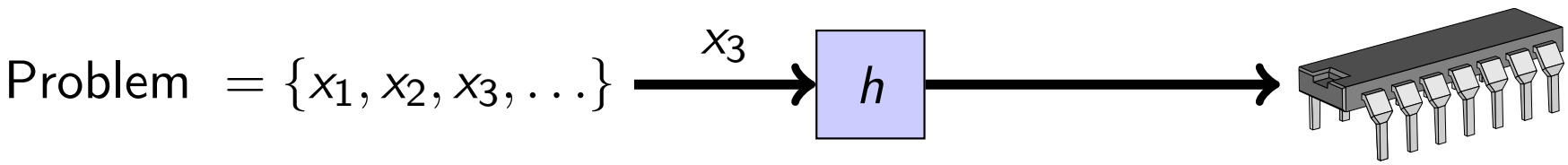
Non-uniform families

$\{$  ,  ,  ,  , $\ldots$ $\}$

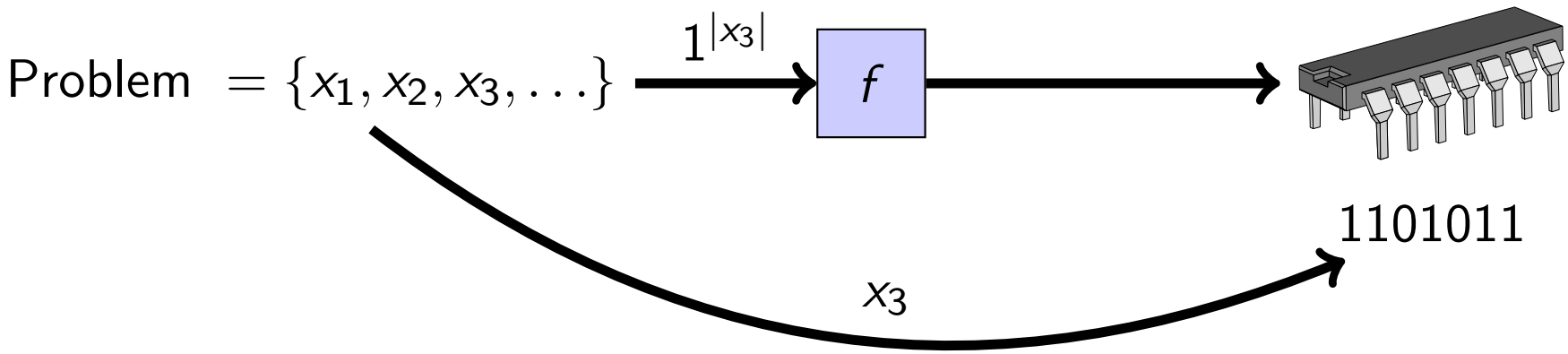
Uniform families

$\left\{ \right.$  $, \ldots \left. \right\}$

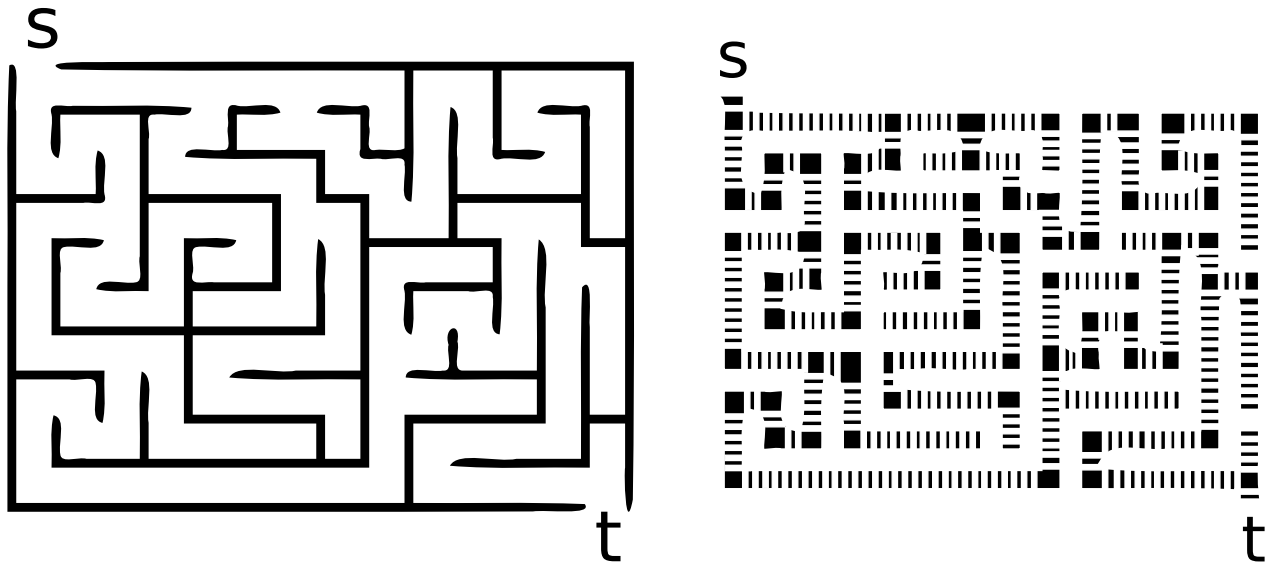
Semi-uniformity



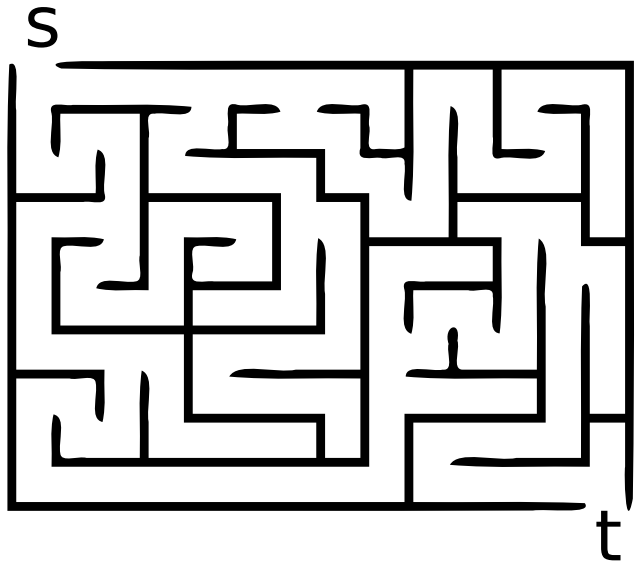
Uniform families

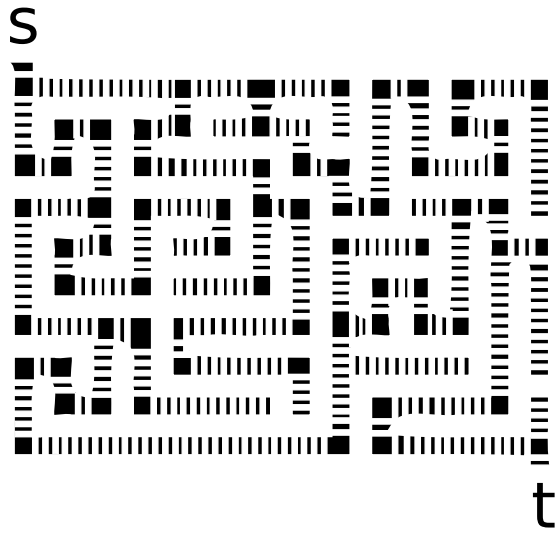


Uniform versus Semi-uniform

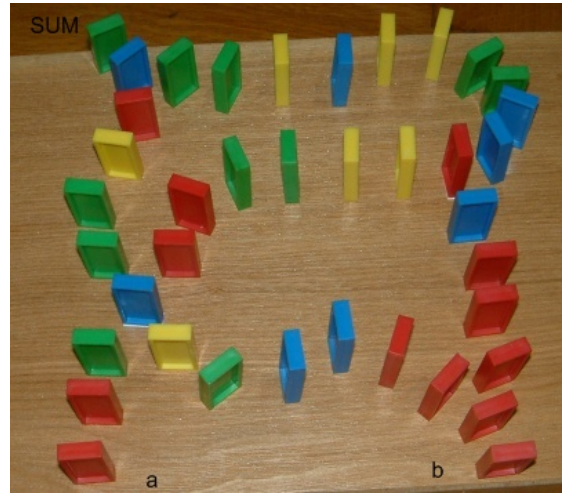


Uniform versus Semi-uniform





$XOR : \{00, 01, 10, 11\}$

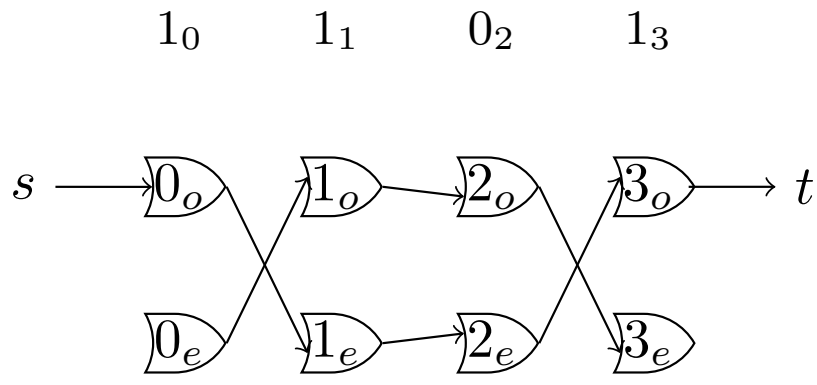


Semi-uniformity is not equal to Uniformity

Theorem

FAC^0-*semi-uniform*-**OR** $\neq$ **FAC**^{0}-*uniform*-**OR**

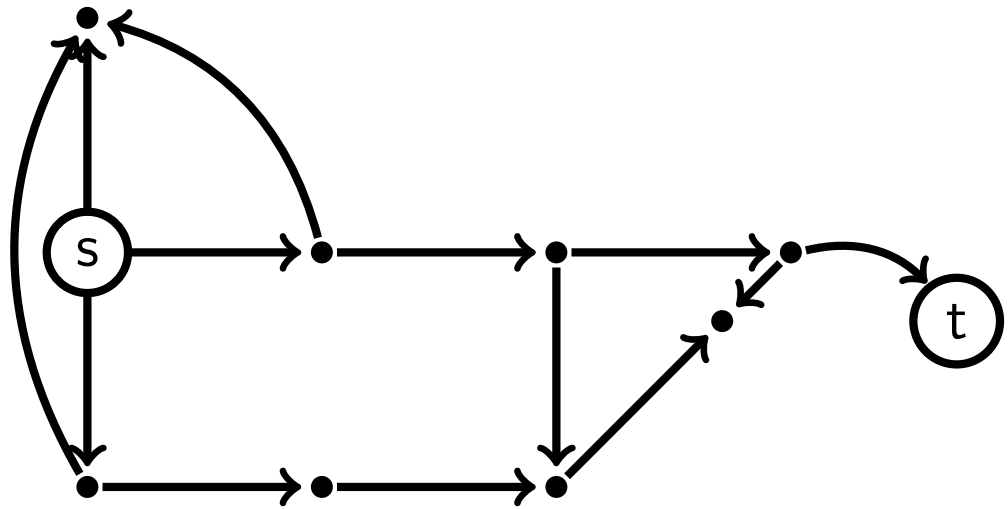
PARITY $\in$ **FAC**^{0}-semi-uniform-**OR**



- PARITY $\notin$ non-uniform **OR**
- $\Longrightarrow$ PARITY $\notin$ **FAC**^{0}-uniform-**OR**

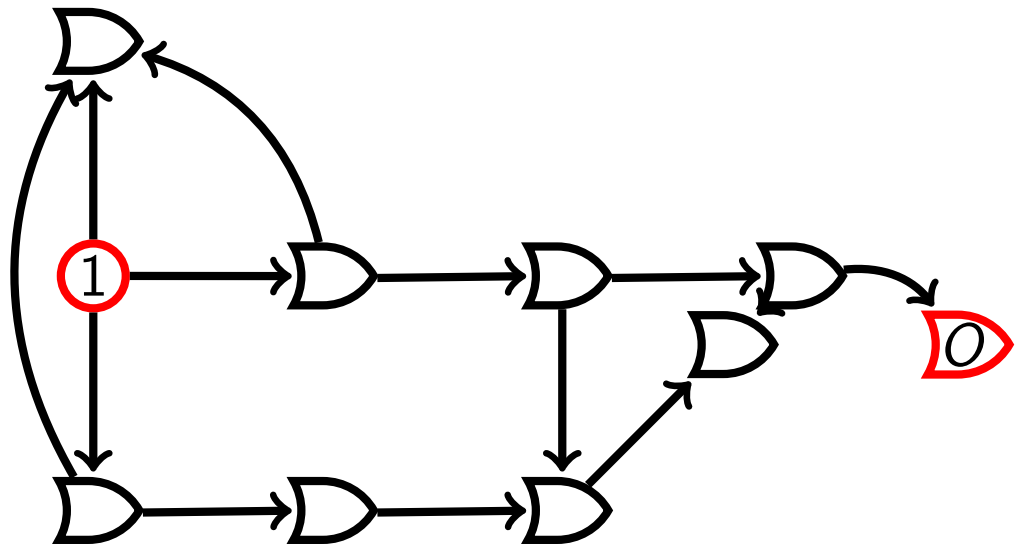
$\mathbf{FAC}^0$-semi-uniform-**OR** = **NL**

PATH $\in$ $\mathbf{FAC}^0$-semi-uniform-**OR**

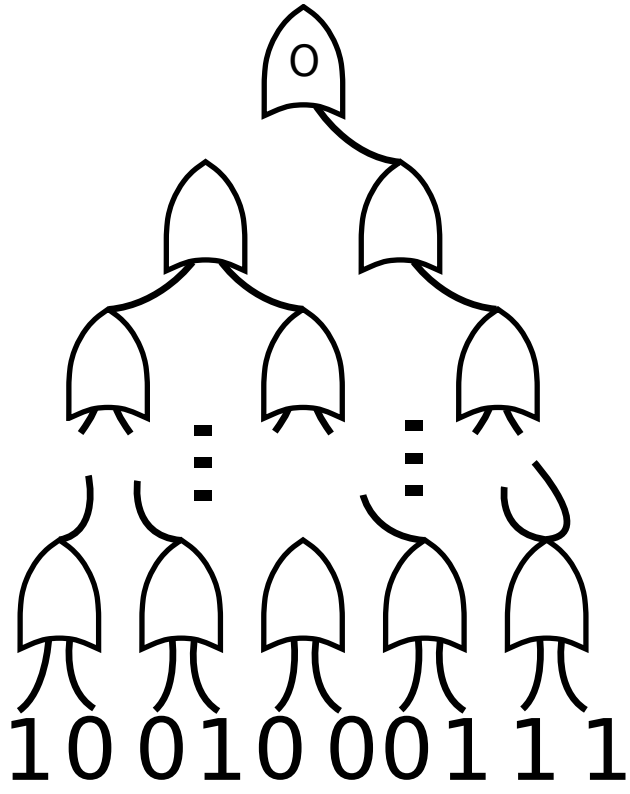


$\mathbf{FAC}^0$-semi-uniform-**OR** = **NL**

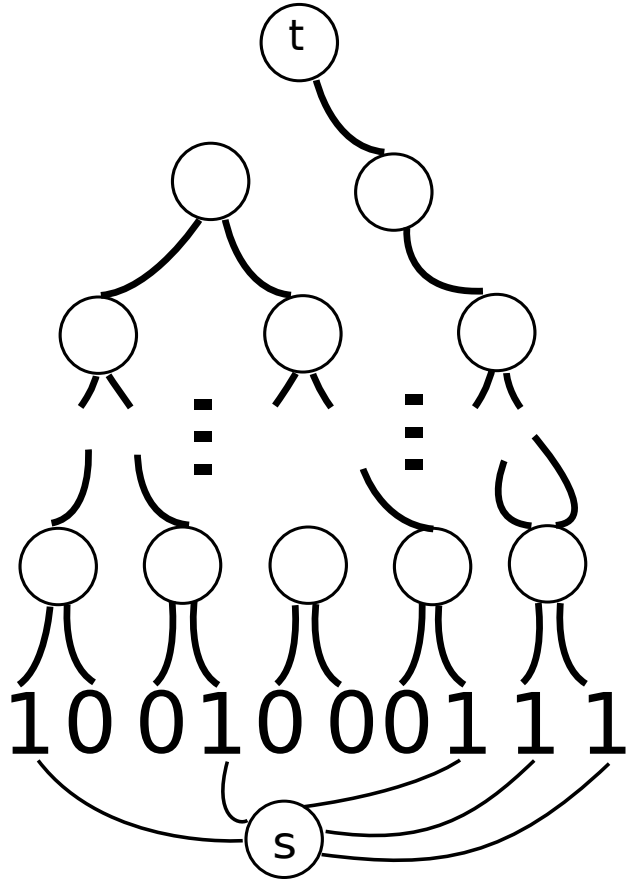
PATH $\in$ $\mathbf{FAC}^0$-semi-uniform-**OR**



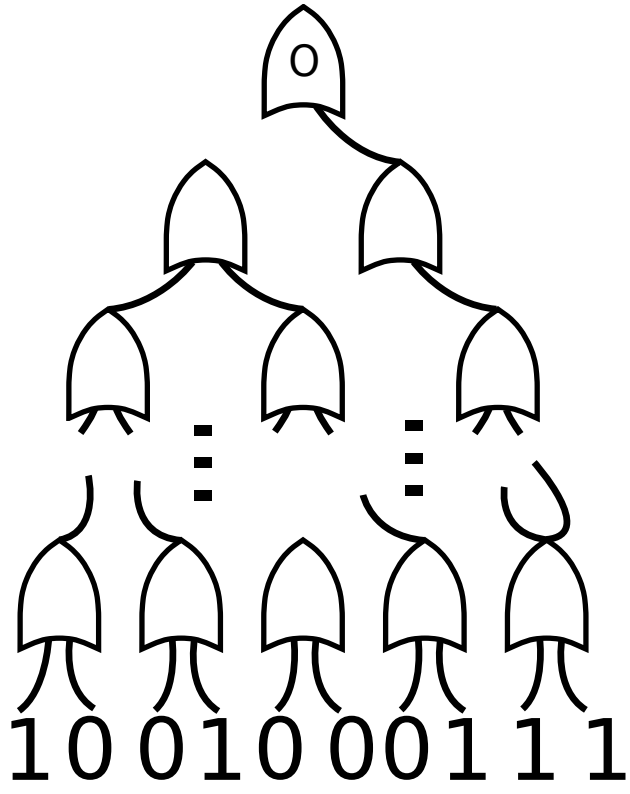
$\mathbf{FAC}^0$-semi-uniform-$\mathbf{OR} \in \mathbf{NL}$



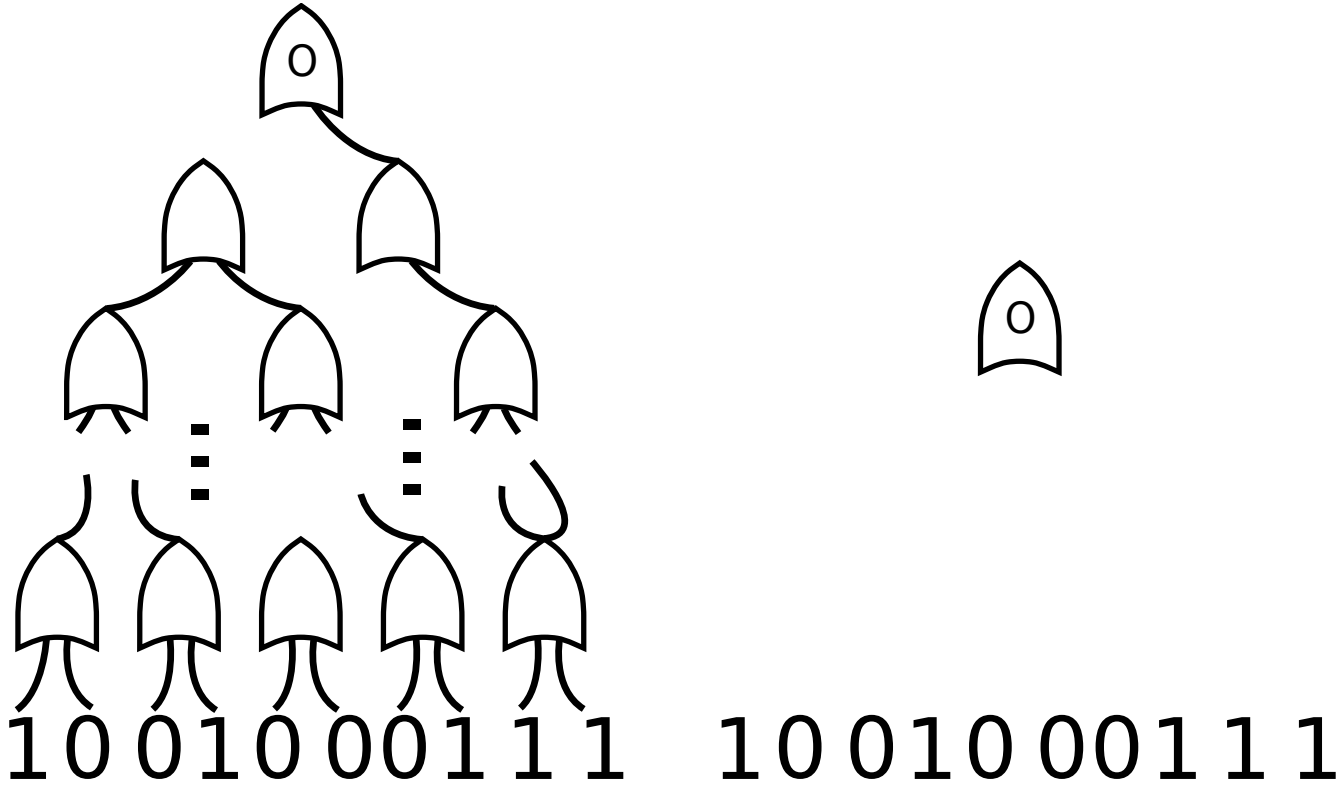
$\mathbf{FAC}^0$-semi-uniform-$\mathbf{OR} \in \mathbf{NL}$



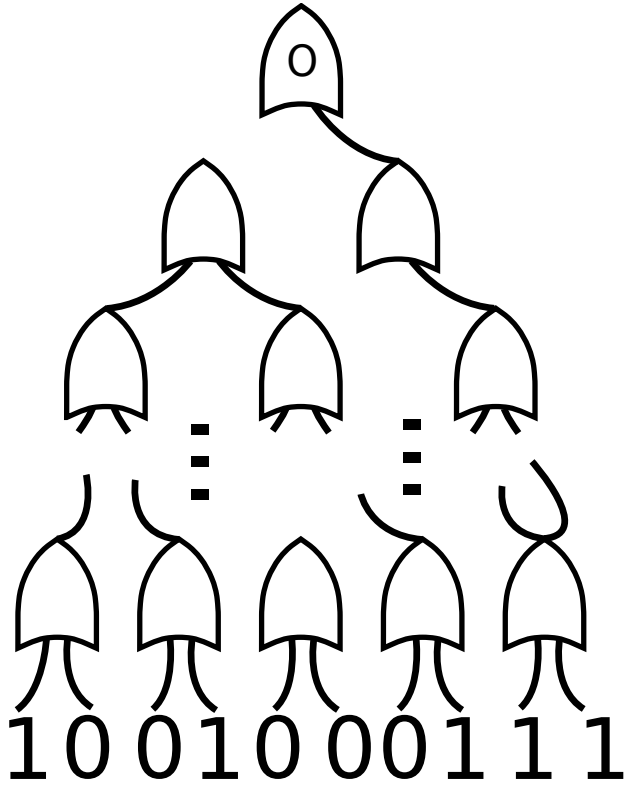
What about **FAC**^{0}-uniform-**OR**

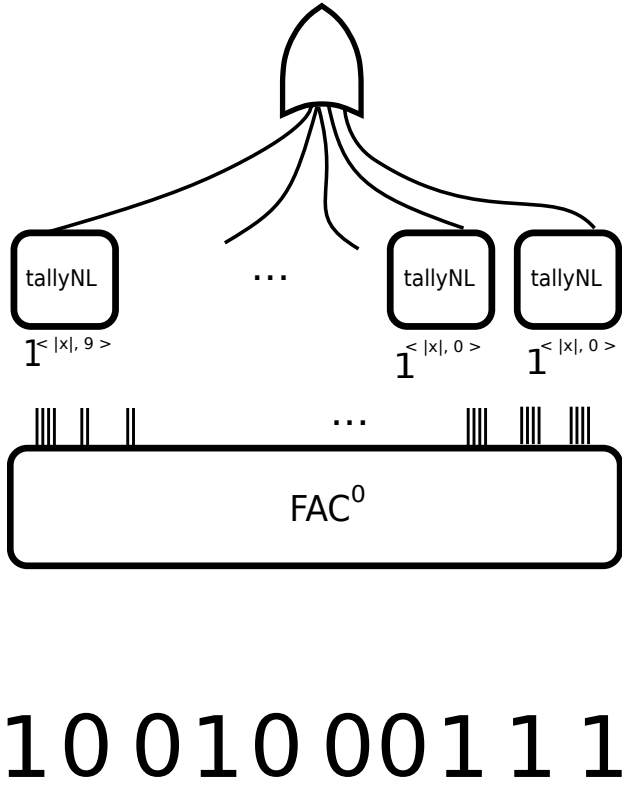


The upper bound



The upper bound





Theorem

$\mathbf{FAC^0}\text{-}uniform\text{-}\mathbf{OR} \subseteq R^{\mathbf{FAC^0}}_{dtt}(\mathbf{tallyNL})$

The lower bound

Theorem

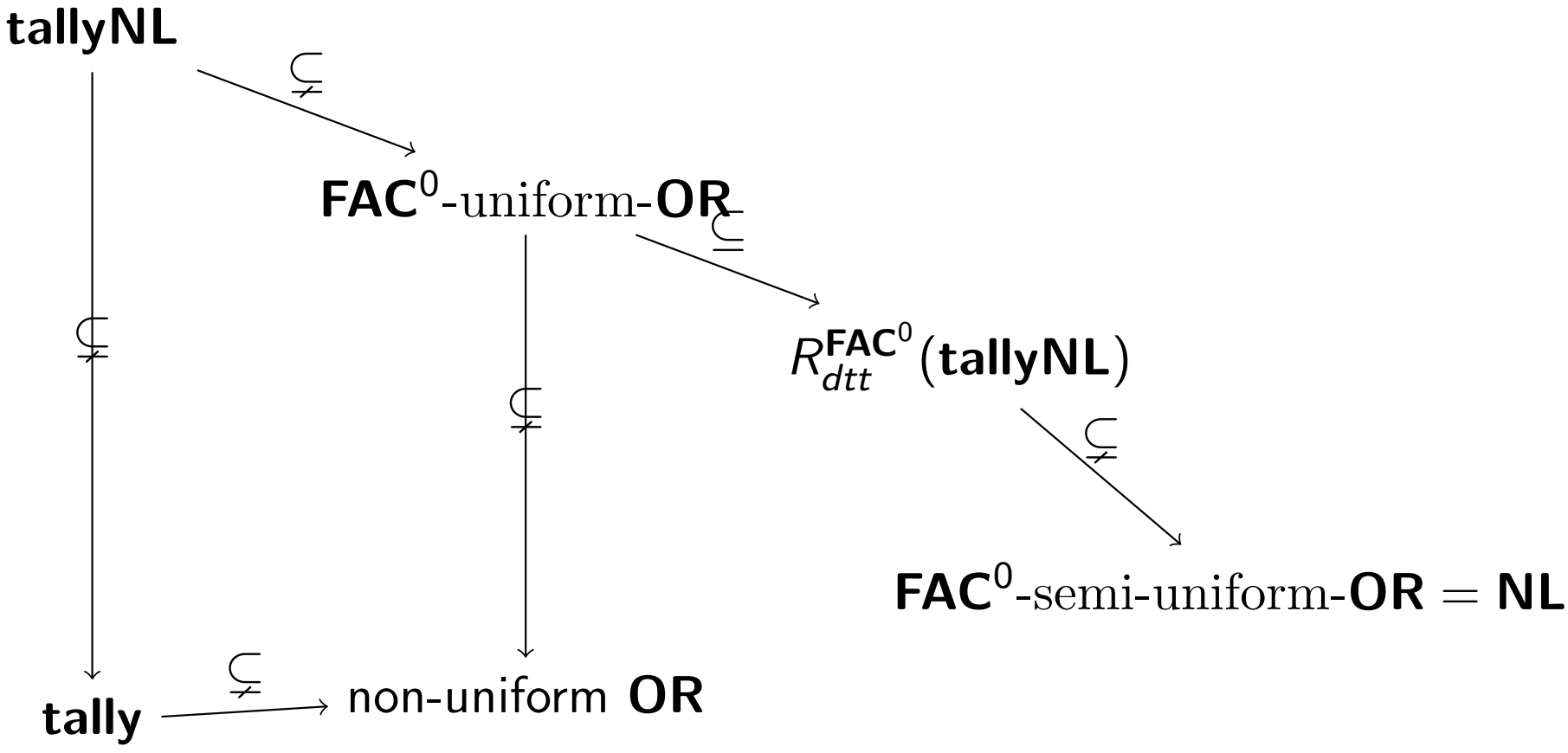
tallyNL $\subsetneq$ $\mathbf{FAC}^0$-$uniform$-**OR**

- M is a **tallyNL** machine.
- $C_M(x)$ constructs a configuration graph for M on x.
- if M accepts on x then $C_M(x)$ is a graph with at least one path from "initial" to "accepting" nodes.
- C'_M gives the same graph as C_M but where each node is an OR gate.
- Use C'_M as the uniformity condition for an **OR** circuit.

Theorem

$R_m^{\mathbf{FAC}^0}$(**tallyNL**) $\notin$ $\mathbf{FAC}^0$-$uniform$-**OR**

Complexity class diagram



Other gates

Theorem

$\mathbf{FAC}^0$-$semi$-$uniform$-**NAND** $= P =$ $\mathbf{FAC}^0$-$uniform$-**NAND**

- **AND** circuits (nearly done)
- **XOR** circuits

Summary

- Uniformity is *strictly weaker* than semi-uniformity
- Result is relevant for (m)any other model(s) using uniform families
  - Tile assembly models
  - DNA circuits
  - synthetic biology
  - ...

Future Work

- Exact characterisation of $\mathbf{FAC}^0$-uniform-**OR**.
- What about other gates?